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09/754,406	01/02/2001	Songjie Xu	APLUS.001A	3824

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EXAMINER	
HOGAN, MARY C	
ART UNIT	**PAPER NUMBER**
2123	6

DATE MAILED: 05/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/754,406	XU, SONGJIE	
	Examiner	Art Unit	
	Mary C Hogan	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06/25/02*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01/02/01* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This application has been examined.

2. Claims 1-31 have been examined and rejected.

Response to Amendment

3. The amendment filed 6/25/2002 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: Substantial portions of the specification have been deleted from the specification and substantial blocks of completely new text have been added to the specification. In both instances, this constitutes new matter. Applicant is required to cancel the new matter in the reply to this Office Action.

Information Disclosure Statement

4. It is requested that a complete copy of the following document be submitted for consideration: Singh, K. J. "Performance Optimization of Digital Circuits", Ph.D. Dissertation, University of California at Berkley, 1992. Pages 33-79 of this document submitted with this application have been considered.

Drawings

5. **Figure 2** should be designated by a legend such as --Prior Art-- because only that which is old is illustrated (**See Specification, paragraph 0014, page 4**). See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. **Claims 1-31** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contain subject matter which was not described in the

specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. For example, "each time decremented by a constant value" (specification, page 20, line 20), and "The critical fanins of node *v*..." (specification page 22, lines 4-10) as well as other subject matter determined to be new matter as discussed above (paragraph 3), were not taught in the original specification therefore, it is not reasonably conveyed to one of ordinary skill in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. **Claims 1-14, 18-21, and 25** are rejected under 35 U.S.C. 102(b) as being anticipated by Singh (Singh, K.J., "Performance Optimization of Digital Circuits, Ph.D. Dissertation, University of California Berkley, 1992), herein referred to as **Singh '92**.

10. As to **Claim 1**, **Singh '92** teaches a method of reducing circuit timing delays comprising

a. selecting a first node **(page 47, first line, "node i")**

b. sorting fanins of the first node according to slack values associated with the corresponding fanins, wherein at least a portion of the slack values differ in value **(page 48-49, description of ∈-critical network and Figure 3.7)**

c. reducing delays associated with fanins having relatively larger negative slack values before reducing delays associated with fanins having relatively smaller negative slack values **(page 50-51 Proof)**

11. As to **Claims 2 and 3**, **Singh '92** teaches reducing delays performed recursively wherein recursively reducing delays is performed until delays cannot be further reduced or timing constraints are violated **(Figure 3.5)**

12. **As to Claim 4**, **Singh '92** teaches selecting the first node comprising

d. performing a timing analysis on a circuit **(page 36, Figure 3.1)**

e. determining a delay target based at least in part on the timing analysis **(page 47, equation 3.1)**

f. determining a slack value for each critical node of the circuit based on the delay target **(page 48, equation 3.2)**

g. sorting the critical nodes based on the corresponding slack values **(pages 50-51, Proof)**

13. As to **Claim 5**, **Singh '92** teaches selecting the first node further comprising selecting a critical node having the largest negative slack **(page 49, "most critical output, O_1")**.

14. As to **Claim 6**, **Singh '92** teaches a method of reducing circuit timing delays comprising

h. selecting a first node **(page 47, first line, "node i")**

i. identifying critical fanins of the first node **(page 48-49, description of ϵ-critical network and Figure 3.7)**

j. recursively reducing delays associated with at least a portion of the critical fanins of the first node **(page 50, Figure 3.8 and accompanying description)**

15. As to **Claim 7**, **Singh '92** teaches recursively reducing delays is performed on critical fanins having relatively larger negative slack values before reducing delays associated with fanins having relatively smaller negative slack values **(page 50-51 Proof)**.

16. As to **Claim 8**, **Singh '92** teaches performing a local transformation on the first node if the reducing delays for at least one of the critical fanins is not successful **(page 51, lines 2-5)**.

17. As to **Claim 9**, **Singh '92** teaches a method of performing circuit delay reduction comprising

k. performing a timing analysis on a circuit **(page 36, Figure 3.1)**

l. determining a delay target based at least in part on the timing analysis **(page 47, equation 3.1)**

m. selecting a first output having a negative slack based at least in part on the delay target **(page 49, "most critical output, O_1")**

n. performing local transformations on transitive fanins of the first output to improve the negative slack **(page 49, lines 12-13)**

18. As to **Claim 10**, **Singh '92** teaches the first output is a critical output **(page 49, "most critical output, O_1")**.

19. As to **Claim 11**, **Singh '92** teaches a method of reducing delays for a circuit having primary input (PI) nodes, at least one primary output (PO) node and a set of circuit nodes between the PI nodes and the PO nodes **(page 57, lines 2-4)**, the method comprising

o. identifying a first critical path between a first PI node and a first PO node that needs to be reduced in delay so as to make it meet a target timing constraint **(page 60, Heuristic-2, first two sentences)**

p. beginning at the first PO node, attempting to reduce a delay associated with a first circuit node **(page 60, Heuristic-2, third sentence)**

q. determining if the delay reduction meets a first predetermined criteria **(page 60, Heuristic-2, forth-sixth sentences)**

20. **Singh '92** teaches identifying a following circuit node in the critical path if the predetermined criteria is not met, attempting to reduce a delay associated with the following circuit node and repeating the steps until the delay cannot be reduced or a set of timing constraints are violated **(page 60, Heuristic-2, sentences five and six, Figure 3.12 (b) and accompanying description)**.

21. As to **Claim 12**, it is noted that the procedure for reducing a delay associated with the second PO node follows the same procedure as reducing a delay associated with the first circuit node described in paragraph 14 and 15. When some other output becomes more critical, it is implied by the discussion **(page 60, Heuristic-2)** that the simulation moves on to the second critical path and reduces the delay based on the improvement in sentence 4.

22. As to **Claim 13**, **Singh '92** teaches the critical path is reduced in delay **(page 60, Heuristic-2, first 3 sentences)** so as to meet a target timing constraint **(page 60, Heuristic-2, 4th sentence)**.

23. As to **Claim 14**, **Singh '92** teaches the criteria for delay improvement **(page 60, Heuristic-2, 4th sentence)**.

24. As to **Claim 18**, **Singh '92** teaches the first PI node and the second PI node are the same **(page 61, Figure 3.12b paths {T,U,W,Y} and {T,Z,V,X})**.

25. As to **Claim 19**, **Singh '92** teaches the first PO node and the second PO node are the same **(page 61, Figure 3.12c paths {U,X} and {V,X})**.

26. As to **Claim 20**, **Singh '92** teaches a portion of the first critical path overlays a portion of the second critical path **(page 67, Figure 3.15, paths {S,U,V,X,Y} and {T,U,V,X,Y})**.

27. As to **Claim 21**, **Singh '92** teaches a method of dynamically reducing delays on a critical path of a circuit topology, the method comprising

r. identifying a critical path of the circuit topology **(page 57, lines 2-3)**

s. selecting a delay target for a primary output associated with the critical path **(page 55, equation 3.3)**

t. reducing a first critical path delay beginning at a first node in closer proximity to a primary input associated with the critical path than to the primary output **(page 58, lines 4-12, n2 is closer to the primary input)**

u. storing the reduced delay **(page 59, Figure 3.11, Δ)**

v. reducing a second critical path delay beginning at a second node located between the first node and the primary output based at least in part on the stored delay **(page 59, Figure 3.11)**

28. As to **Claim 25**, **Singh '92** teaches a layout-driven synthesis design flow comprising

w. selecting a desired circuit delay associated with a first output of a circuit path and calculating an initial circuit delay associated with the first output **(Page 50, Figure 3.8, $s^* = s(O_1)- \epsilon$)**

x. iteratively reducing the initial circuit delay to achieve the desired circuit delay **(Page 50, Figure 3.8, do/while loop)**

29. **Claims 29-31** are rejected under 35 U.S.C. 102(b) as being anticipated by Singh et al (Singh et al, "Timing Optimization of Combinational Logic", Computer-Aided Design, 1988. ICCAD-88. Digest of Technical Papers., IEEE International Conference, 7-10 Nov. 1988, Pages:282 – 285) herein referred to as **Singh '88**.

30. As to **Claim 29**, **Singh '88** teaches a method of performing a local transformation on a node in a circuit topology having at least one fanin cone and a critical fanin cone **(page 282, section 2.1, last paragraph)**, the method comprising

x. identifying a delay target for the node **(page 283, Figure 2, "delay decreases" or "timing constraints not satisfied")**

y. collapsing the critical fanin cone for the node based on a predetermined collapse depth **(page 283, Figure 2, partial collapse function with "d" as an input)**

z. determining if the delay target for the node is met **(page 283, Figure 2, "delay decreases", "timing constraints not satisfied")**

aa. collapsing a fanin cone for the node based on the predetermined collapse depth if the delay target for the node is not met **(page 283, Figure 2, reiteration of the function)**

31. **As to Claim 30**, **Singh '88** teaches an arbitrary value for depth, d **(page 284, section 3, definition of "d")**. It is concluded that a value of two can be used as an arbitrary value for depth and can be changed to three if the value of the delay target is not met.

32. As to **Claim 31**, **Singh '88** teaches performing timing-driven decomposition on the node prior to determining if the delay target is met **(page 283, Figures 2 and 4, page 284, Figure 8)**.

Claim Rejections - 35 USC § 103

33. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

34. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

35. **Claims 15-17, 22-24 and 26-28** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Singh '92** as applied to **Claims 11, 21 and 25** above, and further in view of Applicant's Own Admission, herein referred to at **AOA**.

36. As to **Claims 15-17, 22-24 and 26-28, Singh '92** teaches a method of reducing timing delays on a critical path of a circuit topology during an early stage of the design process **(page 33, paragraph 1)**.

37. **Singh'92** does not explicitly teach the circuit topology being associated with a standard cell design process, a gate array design process or a programmable logic design process and does not specify that the stages of the design process may include the logic optimization phase, the mapping phase or the layout phase.

38. However, **AOA** states in the "Description of Related Technology" that timing problems are becoming more and more crucial in integrated circuit (IC) designs and because of such, timing-driven logic resysthesis is often needed at various design stages to minimize circuit delays **(specification, page 1, paragraph 0003, first sentence)**.

39. "Integrated circuit designs" include circuit topology being associated with a standard cell design process, a gate array design process or a programmable logic design process. Furthermore, "various design stages" include the logic optimization phase, the mapping phase or the layout phase.

40. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the method of reducing timing delays as taught in **Singh '92** for circuit topology being associated

with a standard cell design process, a gate array design process or a programmable logic design process in various design stages including the logic optimization phase, the mapping phase or the layout phase as disclosed in **AOA** since timing-driven logic resynthesis is needed in IC designs at various design stages to minimize circuit delays as stated in **AOA (specification, page 1, paragraph 0003, first sentence)**.

Conclusion

41. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary C. Hogan whose telephone number is 703-305-7838. The examiner can normally be reached on 7:30AM-5PM Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703-305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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